UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,048	04/08/2004	Sadanand V. Deshpande	FIS920030397US1	3047

29154 7590 07/14/2008

FREDERICK W. GIBB, III
Gibb & Rahman, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
07/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,048	DESHPANDE ET AL.	
	Examiner	Art Unit	
	JOHN C. INGHAM	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,7,9,12-14 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,9,12-14 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed 28 April 2008 have been entered.

Claim Objections

2. Claims **13, 14 and 27** are objected to because of the following informalities: claims 13 and 27 depend from cancelled claims 3 and 4. Claim 14 does not have a claim from which it depends. Claim 14 is interpreted to depend from claim 1. Claim 27 is interpreted to depend from claim 7 to establish antecedent basis for 'said silicide regions'. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims **7 and 27** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites that silicide regions are formed on exposed areas of said oxide layer over said substrate. This seems to be illustrated in figure 8, where silicide item 800 is shown on oxide layer 106. However, the specification

recites that exposed areas of the substrate (¶31, ¶38) are silicided (see also item 926 in Fig 9). The claim is interpreted in light of Figure 8.

6. Claim **13** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim recites wherein said oxide layer comprises a low temperature oxide (LTO). However, the specification does not include this description of the oxide layer. Instead the specification recites that the etch stop layer is a low temperature oxide. The claim is interpreted in light of the specification, wherein the etch stop layer is an LTO. Therefore claim 13 is interpreted to depend from claim 6.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims **1 and 14** are rejected under 35 U.S.C. 102(b) as being anticipated by Luning (6,506,642).

9. Regarding claims **1 and 14**, Luning discloses in Fig 6 a complementary metal oxide semiconductor (CMOS) device structure comprising: an NFET gate conductor (41) and a PFET gate conductor (42) formed on a substrate (40); a first spacer (60, of

silicon nitride col 2 ln 57) formed on sidewalls of said NFET gate conductor and said PFET gate conductor; first impurity source/drain implant regions 61) formed in said substrate, substantially adjacent to outer edges of said first spacer (61 is aligned to spacers 60, and separated from the gate electrode 41 by distance W_2) formed on said sidewalls of said NFET gate conductor; a second spacer (of silicon nitride col 2 ln 57) formed on sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor (spacer 60 is formed on spacer 44 of gate 42); and second impurity source/drain implant regions, formed in said substrate, substantially adjacent to outer edges of said second spacer (62 is aligned to spacers 60, and separated from the gate electrode 42 by distance W_3) formed on said sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims **2 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning and Fulford (US 6,258,680).

12. Regarding claim **2**, Luning discloses the CMOS device structure of claim 1, but does not disclose: an oxide layer formed directly on said sidewalls of said NFET gate

conductor and said PFET gate conductor, and directly on areas of said substrate not covered by said NFET gate conductor and said PFET gate conductor.

13. Fulford teaches in Fig 12 that an oxide liner is formed directly on sidewalls of transistor gate conductors and also directly on areas of said substrate not covered by said gate conductors, to act as an etch stop so that the spacers can be formed and removed separately (col 8 ln 17-22). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fulford on the device of Luning so that the nitride spacers could be formed and removed separately from the underlying oxides.

14. Regarding claim **6**, Fulford teaches in Fig 12 that an etch stop layer is formed directly on said oxide layer (150 formed directly on 128) formed directly on said sidewalls of said PFET gate conductor to act as an etch stop so that a second set of nitride spacers can be formed (col 9 ln 4-12).

15. Claims **7 and 27** are rejected as best understood under 35 U.S.C. 103(a) as being unpatentable over Luning, Fulford and Gardner (US 5,882,973).

16. Luning and Fulford disclose the CMOS device structure of claim 2, but do not specify silicide regions formed on exposed areas of said oxide layer over said substrate and tops of said NFET gate conductor and said PFET gate conductor. Instead, Luning teaches a cobalt silicide formed directly on exposed areas of the substrate and gate conductors.

17. Gardner teaches in Fig 6 and Fig 7 that exposed areas of an oxide layer over a substrate and tops of gate conductors are silicided with a two step process in order to enhance conductivity (col 8 ln 20). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Gardner on the device of Luning and Fulford in order to enhance conductivity. Luning discloses the cobalt silicide of claim 27.

18. Claims **9 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning and Wu (US 6,730,556).

19. Luning discloses the CMOS device structure of claim 1, but does not specify wherein a first impurity of said first impurity source/drain implant regions comprises arsenic, or wherein a second impurity of said second impurity source/drain implant regions comprises boron. Instead Luning discloses that the first impurity is n-type and the that the second impurity is p-type.

20. Wu teaches that a suitable n-type dopant for CMOS transistors is arsenic, and a suitable p-type dopant for transistors is boron (col 1 ln 64 – col 2 ln 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Wu on the device of Luning since one of ordinary skill in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination yielding no more than predictable results.

21. As best understood, claim **13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Luning, Fulford and Figura (US 5,750,441).

22. Luning and Fulford disclose the CMOS device structure of claim 6 (see objection and 112 rejection above), but do not specify wherein said etch stop layer comprises a low temperature oxide.

23. Figura teaches that an etch stop layer preferably comprises a low temperature oxide so that the formation temperature is low enough to not disturb the previously formed layers (col 2 ln 57). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Figura on the device of Luning and Fulford so as to not disturb the previously formed layer.

Response to Arguments

24. Applicant's arguments with respect to claims 1-2, 6-7, 9, 12-14 and 27 have been considered but are moot in view of the new ground(s) of rejection. However, the argument that Luning discloses source/drain extensions, which are not aligned with the spacers, is not persuasive. It has been held that the use of the term “comprising” leaves a claim open for inclusion of material or steps other than recited in the claims. Ex parte Davis, 80 USPQ 448 (PTO Bd. App. 1948). Use of the term comprising does not exclude the presence of the element. In re Hunter, 288 F. 2d 930, 129 USPQ 25 (CCPA 1961). In this case, Luning discloses source/drain implant regions (Fig 6 item 61 and 62) that are adjacent to outer edges of the spacers as claimed. The inclusion of other regions that are not adjacent to outer edges is not excluded by the claims. Moreover,

the argument towards the formation process of Luning vs. the instant invention is not persuasive since Luning also performs ion implantation of the source/drain regions after formation of the spacers (col 4 ln 25).

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner
Art Unit 2814

/J. C. I./
Examiner, Art Unit 2814

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814